

***Remarks***

The Examiner is thanked for the early indication of allowable subject matter.

Reconsideration of this Application is respectfully requested.

Claims 8 and 16 are sought to be cancelled without prejudice or disclaimer. Applicant reserves the right to prosecute any cancelled claim or broader claims in a continuation application. Claims 1, 9, 11, 12, 17 and 18 are sought to be amended. Claims 19-27 are sought to be added. Claims 1-7, 9-15, and 17-27 are pending in the application, with 1, 12, and 19 being the independent claims. No new matter has been entered by any amendments.

Based on the above amendment and following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

***Rejections under 35 U.S.C. § 102(b)***

Claims 1, 2, 4, 5, 7, 8, and 12-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,100,830 to Dedic ("Dedic"). Applicants traverse these rejections.

Claim 1 recites at least a system comprising a digital section, including...an acceleration system coupled to the first and second driving devices and configured to accelerate the rise and fall times of the first and second drive signals.

Claim 12 recites at least a system comprising a digital section configured to receive digital signals including a means for generating first and second drive signals having substantially equal rise and fall times therefrom and a means for accelerating the rise and fall times of the first and second drive signals.

The Examiner asserts Dedic teaches "an acceleration system (Fig. 11, elements RC11, RC12) coupled to the first and second driving devices (12, 14) and configured to accelerate the rise and fall times of the first and second drive signals (column 13, lines 7-19)."

However, Dedic teaches away from this in the asserted section:

FIG. 11 further includes respective first and second rate-controlled inverter circuits RCI1 and RCI2...Each rate-controlled inverter circuit RCI1 or RCI2 includes a current source transistor 61 or 71...Each rate-controlled inverter circuit RCI1 or RCI2 further includes a current sink transistor 62 or 72...In addition, the current source and current sink transistors 61, 71, 62 and 72 serve to limit the rise and fall rates of the output signals suitably so as to avoid excessively large currents flowing at the input-signal transitions.

Dedic, col. 12, line 54 to col., 13, line 19. In this section, Dedic teaches limiting rise and fall times, which teaches away from accelerating rise and fall times.

Therefore, Applicant respectfully requests that the Examiner either specifically point out where in the applied patent at least these features are taught or suggested, or reconsider and withdraw the rejection. Applicant believes that claims 1 and 12 are now allowable over the applied patent, and that claims 2-7, 9-11, 13-15, and 17-18 are also allowable, at least based on their dependency from claims 1 and 12, respectively.

***New Claims 19-27***

New claim 19 includes one or more features that are similar to the allowable subject matter. Accordingly, Applicant believes this claim, and its dependent claims 20-27, are allowable.

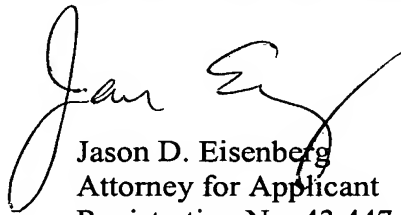
***Conclusion***

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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